CMOS Hex Schmitt Triggers

High-Voltage Types (20-Volt Rating)

■ CD40106B consists of six Schmitt-trigger circuits. Each circuit functions as an inverter with Schmitt-trigger action on the input. The trigger switches at different points for positive- and negative-going signals. The difference between the positive-going voltage (VP) and the negative-going voltage (VN) is defined as hysteresis voltage (VH) (see Fig.6).
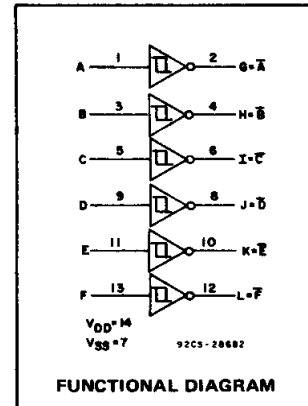
The CD40106B types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

Features:

■ Schmitt-trigger action with no external components
■ Hysteresis voltage (typ.) 0.9 V at V_{DD} = 5 V, 2.3 V at V_{DD} = 10 V, and 3.5 V at V_{DD} = 15 V
■ Noise immunity greater than 50%
■ No limit on input rise and fall times
■ Standardized, symmetrical output characteristics
■ 100% tested for quiescent current at 20 V
■ Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
■ Low V_{DD} to V_{SS} current during slow input ramp
■ 5-V, 10-V, and 15-V parametric ratings
■ Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

■ Wave and pulse shapers
■ High-noise-environment systems
■ Monostable multivibrators
■ Astable multivibrators

FUNCTIONAL DIAGRAM

Fig. 1 — Logic diagram
(1 of 6 Schmitt triggers).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
  Voltages referenced to V_{SS} Terminal) .... –0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS .... –0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT .... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
  For T_A = –55°C to +100°C 500mW
  For T_A = +100°C to +125°C .... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
  FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types).......... 100mW
OPERATING-TEMPERATURE RANGE (T_A) ....–55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ....–65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
  At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max .... +265°C

RECOMMENDED OPERATING CONDITIONS
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A Full Package-Temperature Range)	3	18	V

DYNAMIC ELECTRICAL CHARACTERISTICS
At T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

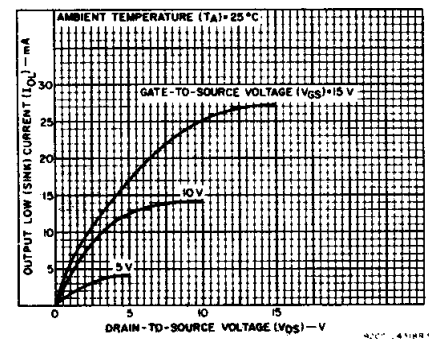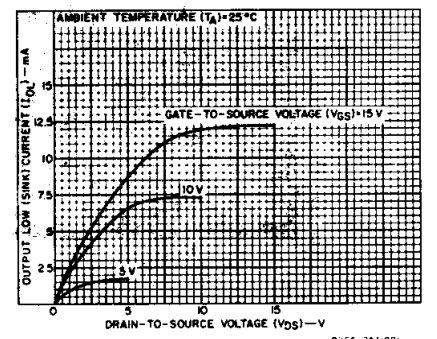| CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS
	V_{DD} (V)	TYP.	MAX.	
Propagation Delay Time:	5	140	280	
t_{PHL},	10	70	140	ns
t_{PLH}	15	60	120	
Transition Time:	5	100	200	
t_{THL},	10	50	100	ns
t_{TLH}	15	40	80	
Input Capacitance, C_{IN}	Any Input	5	7.5	pF

Fig.2 — Typical output low (sink) current characteristics.

Fig.3 — Minimum output low (sink) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) −55	−40	+85	+125	+25 Min.	Typ.	Max.	UNITS
Quiescent Device Current, I_{DD} Max.	—	0,5	5	1	1	30	30	—	0.02	1	µA
	—	0,10	10	2	2	60	60	—	0.02	2	
	—	0,15	15	4	4	120	120	—	0.02	4	
	—	0,20	20	20	20	600	600	—	0.04	20	
Positive Trigger Threshold Voltage V_P Min.	—	—	5	2.2	2.2	2.2	2.2	2.2	2.9	—	V
	—	—	10	4.6	4.6	4.6	4.6	4.6	5.9	—	
	—	—	15	6.8	6.8	6.8	6.8	6.8	8.8		
V_P Max.	—	—	5	3.6	3.6	3.6	3.6	—	2.9	3.6	
	—	—	10	7.1	7.1	7.1	7.1	—	5.9	7.1	
	—	—	15	10.8	10.8	10.8	10.8	—	8.8	10.8	
Negative Trigger Threshold Voltage V_N Min.	—	—	5	0.9	0.9	0.9	0.9	0.9	1.9	—	V
	—	—	10	2.5	2.5	2.5	2.5	2.5	3.9	—	
	—	—	15	4	4	4	4	4	5.8	—	
V_N Max.	—	—	5	2.8	2.8	2.8	2.8	—	1.9	2.8	
	—	—	10	5.2	5.2	5.2	5.2	—	3.9	5.2	
	—	—	15	7.4	7.4	7.4	7.4	—	5.8	7.4	
Hysteresis Voltage V_H Min.	—	—	5	0.3	0.3	0.3	0.3	0.3	0.9	—	V
	—	—	10	1.2	1.2	1.2	1.2	1.2	2.3	—	
	—	—	15	1.6	1.6	1.6	1.6	1.6	3.5	—	
V_H Max.	—	—	5	1.6	1.6	1.6	1.6	—	0.9	1.6	
	—	—	10	3.4	3.4	3.4	3.4	—	2.3	3.4	
	—	—	15	5	5	5	5	—	3.5	5	
Output Low (Sink) Current, I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	—	
	2.5	0.5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	—	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	—	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	—	
Output Voltage Low-Level, V_{OL} Max.	—	5	5	0.05				—	0	0.05	V
	—	10	10	0.05				—	0	0.05	
	—	15	15	0.05				—	0	0.05	
Output Voltage High Level, V_{OH} Min.	—	0	5	4.95				4.95	5	—	
	—	0	10	9.95				9.95	10	—	
	—	0	15	14.95				14.95	15	—	
Input Current, I_{IN} Max.	—	0,18	18	±0.1	±0.1	±1	±1	—	$\pm 10^{-5}$	±0.1	µA

Fig.4 — Typical output high (source) current characteristics.
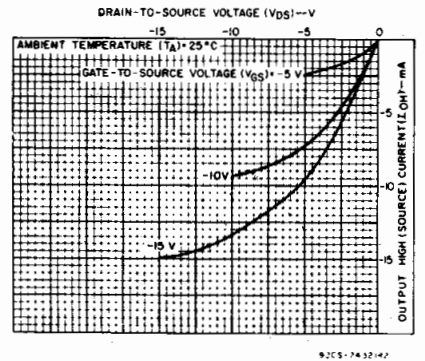
Fig.5 — Minimum output high (source) current characteristics.

Fig.7 — Input and output characteristics.

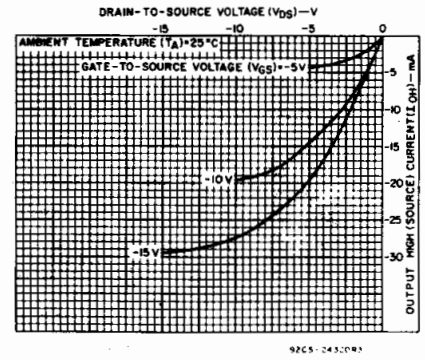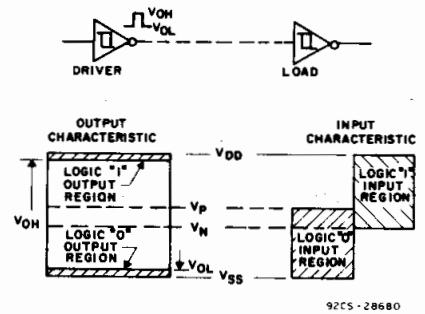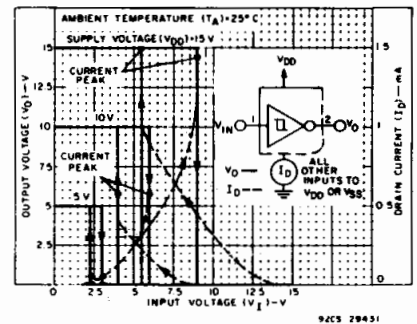a) Definition of V_P, V_N, V_H

b) Transfer characteristics of 1 of 6 gates

Fig.6 — Hysteresis definition, characteristics, and test set-up.

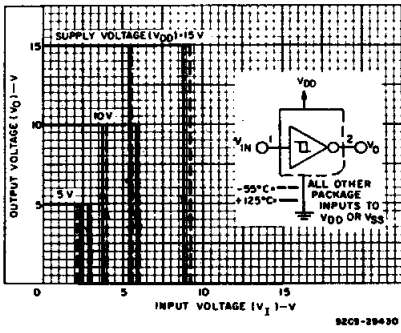Fig.8 — Typical current and voltage transfer characteristics.

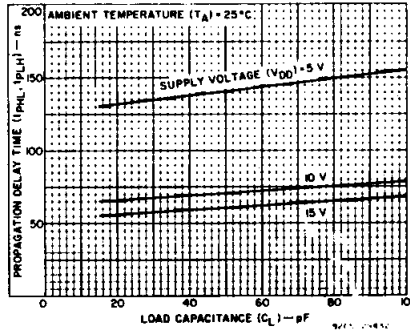Fig.9 — Typical voltage transfer characteristics as a function of temperature.

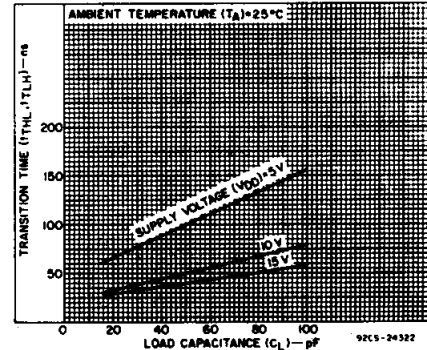Fig.10 — Typical propagation delay time as a function of load capacitance.

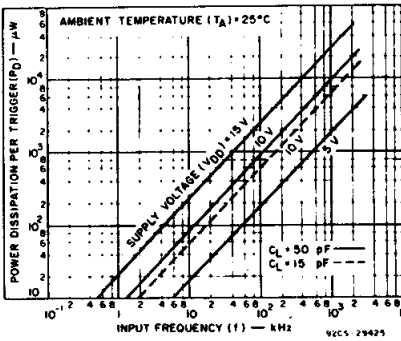Fig.11 — Typical transition time as a function of load capacitance.

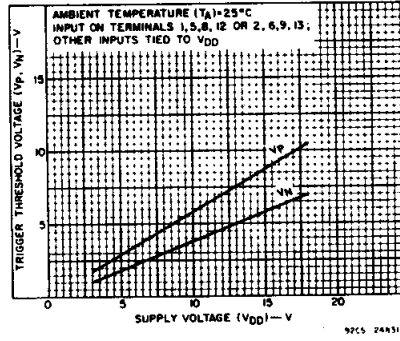Fig.12 — Typical power dissipation per trigger as a function of input frequency.

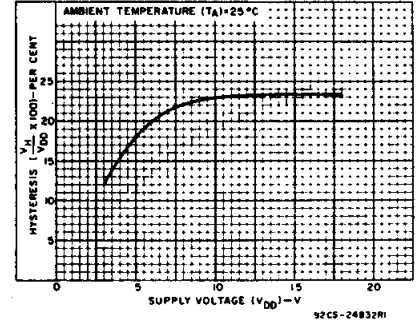Fig.13 — Typical trigger threshold voltage as a function of supply voltage.

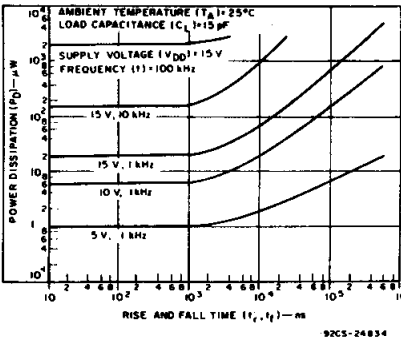Fig.14 — Typical per cent hysteresis as a function of supply voltage.

Fig.15 — Typical power dissipation as a function of rise and fall times.
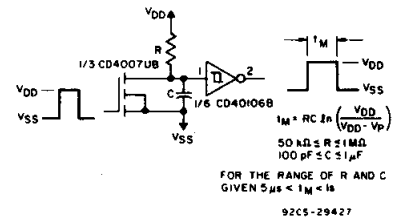
APPLICATIONS
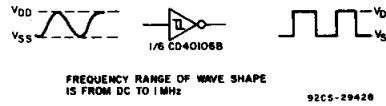
Fig.16 — Wave shaper.

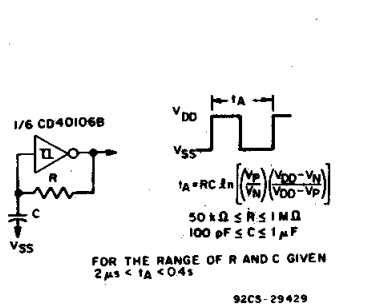Fig.17 — Monostable multivibrator.
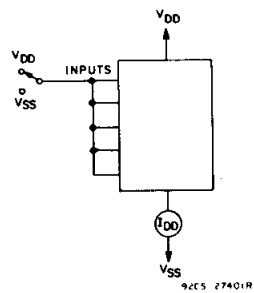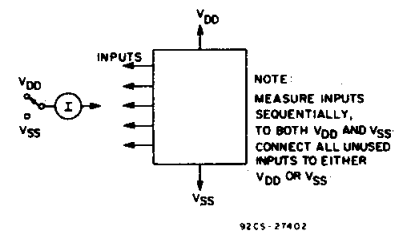

Fig.18 — Astable multivibrator.

Fig.19 — Quiescent device current test circuit.

Fig.20 — Input current test circuit.